FPGA IMPLEMENTATION OF DIGITIZED PHASE-LOCKED LOOP WITH TOLERANCE TO PVT VARIATIONS

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Abstract— A spread-spectrum clock generator (SSCG) is realized by an under-damping all-digital phase-locked loop (PLL). In this SSCG, the spread spectrum clocking is achieved by switching the divider without a delta-sigma modulator. By using a digital self-calibration technique, the frequency of this SSCG has a triangular modulation and relaxes the process variations. This SSCG is fabricated in a 0.18m CMOS process. The measured electro-magnetic interference reduction is 14.32dB. The measured rms and peak-to-peak jitters are 1.43ps and 13.31ps in a PLL mode, respectively. The measured rms and peak-to-peak jitters are 2.65 ps and 19.86ps in a spreadspectrum modulation, respectively.

Index Terms— Phase ed loop(PLL),Spread Spectrum Clock generator(SSCG), Convolutional coding, BCH coding, adaptive quantizers. lock

1 INTRODUCTION

A phase-locked loop or phase locked loop is a control system that generates an output signal whose phase is related to the phase of an input signal. While there are several differing types, it is easy to initially visualize as an electronic circuit consisting of a variable frequency oscillator and a phase detector. The oscillator generates a periodic signal[1]. The phase detector compares the phase of that signal with the phase of the input periodic signal and adjusts the oscillator to keep the phases matched. Bringing the output signal back toward the input signal for comparison is called a feedback loop since the output is 'fedback' toward the input forming a loop. Keeping the input and output phase in lock step also implies keeping the input and output frequencies the same. For all-digital methods, the matching requirements for the delay cells in the delay line limit the accuracy of the frequency modulation profile. The self-calibration will be also needed. A self-calibration circuit calibrates the SSCG in the background to relax the pressuress, voltage, and temperature (PVT) variations.

2 BASICS OF PHASE LOCKED LOOP

The Phase Locked Loop has three main blocks. It includes Phase detector, Loop filter and Voltage controlled oscillator as shown in fig.1. Phase detector compares between input and DCO output signal. Output depends upon the phase error. Output signal contains low frequency and higher frequency component. Loop filter is simply act as a integrator.

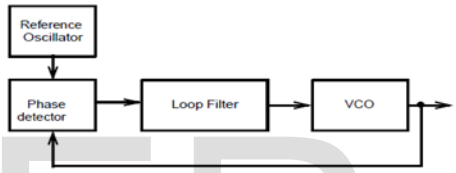

Figure 1. Basic layout of phase locked loop

Voltage Controlled Oscillator is treated as a linear, time-invariant system. Excess phase of the VCO is the system output. Output frequency can be changed by changing the output of the loop filter.

3 TYPES OF PLL

PLL includes five types.They are analog phase-locked loop also referred to as a linear phase-locked loop, digital phase-locked loop, all digital phase-locked loop , software phase-locked loop and Neuronal PLL.

A. Linear PLL:

The Analog or linear PLL has phase detector and loop filter. Phase detector is an analog multiplier. Loop filter is active or passive. Uses a Voltage-controlled oscillator.

B. Digital PLL:

Digital PLL is an analog PLL with a digital phase detector such as XOR, edge-trigger JK, phase frequency detector. May have digital divider in the loop.

C. All Digital PLL:

All digital PLL has Phase detector, filter and oscillator are digital. Uses a numerically controlled oscillator.

D. Software PLL:

Software PLL which includes functional blocks that are implemented by software rather than specialized hardware.

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E. Neuronal PLL:

Neuronal PLL has an Phase detector, filter and oscillator are neurons or small neuronal pools. Uses a rate controlled oscillator .

In this ,All Digital Phase Locked Loop is discussed detailed.

4 ALL DIGITAL PHASE LOCKED LOOP

The All-digital phase locked loop (ADPLL) is a phase lock loop implemented in purely digital circuitry and operating on finite precision digital words. ADPLL has an operating input frequency between 10 kHz to 150 kHz.

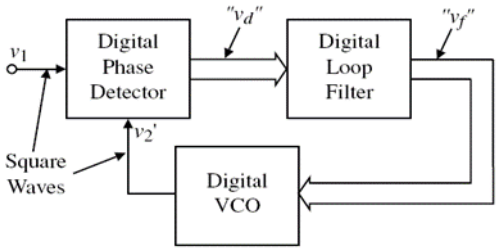

Figure.2. Basic Block Diagram of ADPLL

Output frequency between 10MHz to 300 MHz. Block diagram for All Digital Phase Locked Loop (ADPLL) is shown in Fig.2. ADPLL benefits are digital design regarding area, power consumption, and flexibility. Components of ADPLL includes Digital Phase Detector, Digital loop filter and Digitally Controlled Oscillator.

A.Digital Phase Detector:

The phase frequency detector is a significant aspect of the PLL because it determines whether the reference clock and divided DCO clock are in phase and are running at the same frequency. A modified D Flip-flop was utilized because the D input doesn't change and remains high always. The output of the modified D Flip-flops enters a two input NOR gate that resets the Flip-flops if both clocks are high. The up and down signals indicate if the DCO clock needs to be increased (up is true) or decreased (down is true). The event and direction signal are necessary to create the up and down enable signals for the T2D converter. Additional circuitry between the PFD and T2D is required for the signal conversion to takes place.

B.Digital Loop Filter:

Digital loop filter simplest loop filter. It is always operate in conjunction with EXOR or JK FF phase detector. For getting clock and direction signal a pulse forming circuit is used. Counter is incremented on each UP pulses and it is decremented on each down signals .So counter adds both pulses .So its work like an integrator. Loop filter has has two counters .Both are independent .One is called Up and other is Down counter .But both counts in upward direction. Counter has modulus k. So counter contents has range from 0 to k-1.Couter clock frequency is M times multiple of center frequency. M has typical values of 8, 16, 32….Down counter is enabled when DN/UP has logic high and up counter is enabled when this logic low value. When contents exceed k-1 both counters resets. "Carry" is MSB of the Up counter .The "borrow" signal is MSB of the Down counter. When Up-counter stored data ≥ k/2 "carry" is high .When down counter stored data≥ k/2 "borrow" is high. Frequency of DCO is controlled by positive edges of the signal.

C.Digitally Controlled Oscillator:

Digitally Controlled oscillators are nothing but a modified oscillator. Depending upon output of the loop filter they change their frequency. Divide by N counter DCO and Increment-decrement counter are the types of DCO. A simple÷N counter works as DCO. High frequency signal operates at very high frequency. Divide by N counter produces N bit parallel output. Drawback is that it can't design jitter. Increment-Decrement Counter consists of two blocks. Carry is assigned to DECR input and Borrow is assigned to INCR input. ID counter with ÷ N counter for again dividing the OUT. Clock of increment-decrement counter is 2N times multiple of center frequency.

TABLE I
COMPARISON OF ANALOG AND DIGITAL PLL

Parameter	Digital PLL	Analog PLL
Power	5.883 dBm	3.5 dBm
Lock time	1.5us(100-120 cycles)	10us
Jitter/Phase Noise	0.4ns	-212dBc/Hz

5 JITTER

Jitter is the undesired deviation from true periodicity of anassumedperiic signal in electronics and telecommunications often in relation to a reference clock source. Jitter may be observed in characteristics such as the frequency of successive pulses, the signal amplitude, or phase of periodic signals. Jitter is a significant, and usually undesired, factor in the design of almost all communications links (e.g., USB,PCIe, SATA, OC-48).In clock recovery applications it is called timing jitter. Jitter can be quantified in the same terms as all time-varying signals, e.g., RMS, or peak-to-peak displacement. Also like other time-varying signals, jitter can be expressed in terms of spectral density (frequency content). The waveform for Jitter is shown in figure 3. Jitter period is the interval between two times of maximum effect (or minimum effect) of a signal characteristic that varies regularly with time[3]. Jitter frequency, the more commonly quoted figure, is its inverse. ITU-T G.810classifies jitter frequencies below 10 Hz as wander and frequencies at or above 10 Hz as jitter.

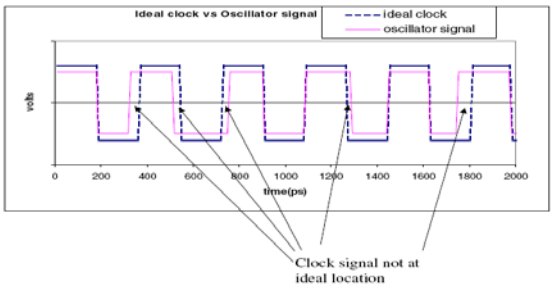

Figure.3. Example of jitter

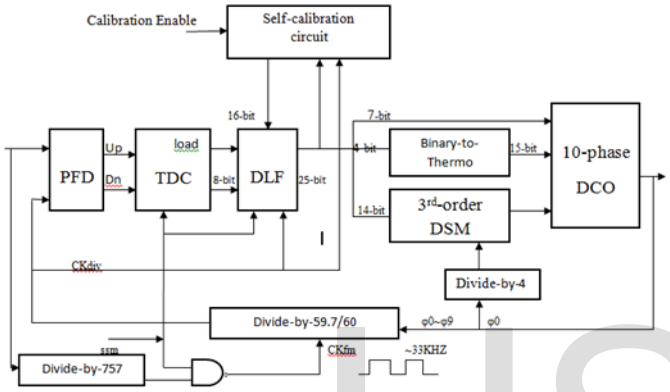

Figure.4. Proposed DPLL with PVT variations.

Frequency Dual-Modulus Divider:

In order to realize a factional division ratio of 59.7, a 10-phase DCO is adopted in this work. The factional dual-modulus divider, which is realized by a divide by (N-1/10)/(N+1/5) divider, a program counter, a swallow counter, and auxiliary digital circuits. When SSM=0,this ADPLL works in a PLL mode and S=4 is selected. When S is equal to 4,the division ratio is 60.The clock is 33KHZ switches values between three and four respectively. This time interval is equal to 200 p for the DCO of 1.5 GHz. Because of this large timing margin of 200 ps, the 10-1 MUX can be realized by conventional static logics.Both are independent .One is called Up and other is Down counter .But both counts .in upward direction. Counter has modulus k. So counter contents has range from 0 to k-1.Couter clock frequency is M times multiple of center frequency. M has typical values of 8, 16, 32….Down counter is enabled when DN/UP has logic high and up counter is enabled when this logic low value. When contents exceed k-1 both counters resets.

Digital Self-Calibration Circuit:

The variations not only affect the down-spreading ratio and triangular modulation profile, but also the loop bandwidth, EMI reduction and jitter performance. Three process corners are considered for NMOS and PMOS devices, fast-fast (FF) corner with 0'c, typical-typical (TT) corner with 27'c, and slow-slow (SS) corner with 80'c. According to simulation results, the simulated parameters Kc and TDC for these three corners are listed.To tolerate the PVT variations, the nature frequency and damping factor should be adjusted. In this work, the proportional and integral gains, Kp and Ki, of the DLF are adjusted by a digital self-calibration circuit to achieve the required the nature frequency and damping factor. The spread spectrum ratio of 5000 ppm. The required Kp and Ki for FF, TT and SS corners are 448 and 2, 1024 and 5 2432 and 13, respectively.

TABLE II
COMPARISON OF SYNTHESIS RESULTS

Technique	Pressure	Volume	Temperature
1st-order DSM	23.4 mW	33KHz	1.5GHz
3rd-order DSM	20 mW	25KHz	1GHz

6 Conclusion

A triangular-wave-modulation SSCGis realized by switching the divider of an ADPLL without a DSM. To reduce the phase jumping step, a 10-phase DCO and a fractional divider are adopted.

Furthermore, the proposed system will be developed using verilog-HDL and FPGA implementation using a self-calibration circuit is also adopted to calibrate the SSCG in the background to tolerate the PVT variations. This chip has been fabricated a 0.12 m CMOS process.

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